AMENDMENTS

IN THE CLAIMS

Please amend the claims as follows:

Please amend claim 1 as follows:

SUB FI

1. (Twice Amended) A method for forming bonding pads of a semiconductor substrate comprising the steps of:

providing top level interconnecting metal for interconnecting lines and top level bond pad metal for bond pads, said interconnecting lines being adjacent to said top level bond pad, said interconnecting lines being adapted to ultra-small line spacing technologies, said top level metal being formed selectively on an insulating film overlying the main surface of a semiconductor substrate in which a desired circuit element is being formed, the surface of said insulating film being partially exposed;

depositing a passivation layer over said top-level metal and over the partially exposed surface of said insulating layer, said passivation layer comprising a first and a second passivation layer;

depositing a layer of photosensitive polyimide over said passivation layer, filling keyholes between closely spaced interconnect lines, thereby eliminating any detrimental effect

caused by accumulation of semiconductor material inside said keyholes and eliminating negative effect that passivation layer imperfections have on device reliability, further preventing etching damage and damage of cracking and delamination to the surface of said passivation layer, further providing a stress buffer to said passivation layer, reducing stress impact on the passivation layer;

patterning and etching said layer of photosensitive polyimide thereby forming a pattern for said bonding pads;

patterning and etching said passivation layer thereby exposing said bond pad, said patterning and etching of said passivation layer to take place after said patterning and etching of said layer of photosensitive polyimide; and

curing and cross-linking said photosensitive polyimide said curing and cross-linking of said photosensitive polyimide to take place after said patterning and etching of said passivation layer.

Please amend claim 8 as follows:

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8. (Twice Amended) The method of claim 1 wherein the thickness of said photosensitive polyimide is within the range of between 5.0 and 9.5 μm after deposition of said photosensitive polyimide whereby shrinkage of up to 40% of said thickness could occur after curing of said layer of photosensitive polyimide, filling

keyholes between closely spaced interconnect lines, thereby eliminating any detrimental effect caused by accumulation of semiconductor material inside said keyholes and eliminating negative effect that passivation layer imperfections have on device reliability, further preventing etching damage and damage of cracking and delamination to the surface of said passivation layer, further providing a stress buffer to said passivation layer, reducing stress impact on the passivation layer, allowing for adopting planarization technology to ultra-small line spacing technology.

Please amend claim 9 as follows:

9. (Amended) The method of claim 1 wherein said patterning said layer of photosensitive polyimide is creating a pattern that [is above and mates] aligns with said plurality of bond pads.

Please amend claim 11 as follows:

11. (Amended) The method of claim 1 wherein said patterning and etching of said photosensitive polyimide is achieved cross-linking with ultra-violet radiation through a mask while masking from UV exposure polyimide regions that [are above and mate] align with said bond pads and further dissolving away in a solvent the non-cross-linked polyimide over the bond pads,

allowing deposition of a thick and cross-linked polyimide film thus preventing etching damage to the passivation layer..

Please amend claim 15 as follows:

15. (Twice Amended) The method of claim 1 wherein said top level metal for interconnecting lines and top level metal for bond pads are formed within or on top of any layer of a semiconductor device other than or in addition to said semiconductor substrate, said interconnecting lines being adjacent to said bond pads, said interconnecting lines being adapted to ultra-small line spacing technologies,

Please amend claim 16 as follows:

16. (Twice Amended) The method of claim 1 wherein said top level metal for interconnecting lines and top level metal for bond pads are formed selectively on the bare main surface of a semiconductor substrate in which a desired circuit element is being formed, said interconnecting lines being adjacent to said top level metal for bond pads, said interconnecting lines being adapted to ultra-small line spacing technologies.

Please amend claim 17 as follows:

17. (Amended) The method of claim 1 wherein said top level metal for interconnecting lines and top level metal for bond pads are formed within or on top of any layer of a semiconductor device other than or in addition to said semiconductor substrate, said interconnecting lines being adjacent to said top level metal for bond pads, said interconnecting lines being adapted to ultra-small line spacing technologies.

Please amend claim 18 as follows:

18. (Amended) The method of claim 1 wherein said top level metal for interconnecting lines and top level metal for bond pads are formed selectively on the bare main surface of a semiconductor, said interconnecting lines being adjacent to said top level metal for bond pads, said interconnecting lines being adapted to ultra-small line spacing technologies.

Please amend claim 20 as follows:

20. (Twice Amended) A method of forming planarized bonding pads within the structure of a semiconductor device comprising the steps of:

providing a semiconductor substrate, said semiconductor substrate to contain electrical circuits or other electrical functional electrical components;

providing a wiring layer having wiring and having a plurality of bond pads having a thickness, the wiring of said wiring layer being directly connected to said bond pads in addition to being connected to said electrical circuits or other electrical functional components within said semiconductor substrate, said wiring layer being adjacent to said plurality of bond pads, said wiring of said wiring layer being adapted to ultra-small line spacing technologies, the wiring layer being formed selectively on an insulating film overlying the main surface of a semiconductor substrate in which a desired circuit element is being formed, the surface of said insulating layer being partially exposed;

depositing a layer of top metal over said bond pads thereby depositing bond pad metal;

depositing a passivation layer over said wiring layer and over said bond pad metal and over the exposed surface of the insulating layer;

depositing a layer of photosensitive polyimide over said passivation layer to a thickness within the range of between 5.0 and 9.5 μm, filling keyholes between closely spaced wiring of said wiring layer, thereby eliminating any detrimental effect caused by accumulation of semiconductor material inside said keyholes and eliminating negative effect that passivation layer imperfections have on device reliability, further preventing

etching damage and damage of cracking and delamination to the surface of said passivation layer, further providing a stress buffer to said passivation layer, reducing stress impact on the passivation layer;

patterning and etching said layer of photosensitive polyimide thereby forming a pattern of photosensitive polyimide, said pattern being identical to the pattern of said bond pads, partially removing said photosensitive polyimide from above the surface of said bond pads;

etching said layer of passivation, thereby removing said passivation from above said bond pads, said patterning and etching of said passivation layer to take place after said patterning and etching said layer of photosensitive polyimide; and

curing and cross-linking said photosensitive polyimide thereby protecting the underlying circuitry, said curing and cross-linking of said photosensitive polyimide to take place after said etching of said passivation layer.

REMARKS

Examiner N. Berezny is thanked for his thorough examination of the Prior Art.